



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/512,119	10/21/2004	Matthias Wendt	DE 020103	2393
24738 7590 04/09/2008 PHILIPS ELECTRONICS NORTH AMERICA CORPORATION INTELLECTUAL PROPERTY & STANDARDS 370 W. TRIMBLE ROAD MS 91/MG SAN JOSE, CA 95131				
			EXAMINER ROSENAT, DEREK JOHN	
			ART UNIT 2834	PAPER NUMBER
			MAIL DATE 04/09/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/512,119

Applicant(s)

WENDT ET AL.

Examiner

Derek J. Rosenau

Art Unit

2834

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 January 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 10 and 12-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 10, 12-22 and 26 is/are rejected.
- 7) ☒ Claim(s) 23-25 and 27-30 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB008)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Appeal Brief

1. In response to the Appeal Brief filed 7 January 2008, prosecution of this application is reopened. With respect to claims 10 and 12-22, the grounds of rejection remain the same; however, clarifications of those grounds of rejection are made herein. With respect to claim 26, the grounds of rejection are being changed to include both Sakurai and Sakurai et al.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 10, 12-22, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakurai (US 4965532) in view of Sakurai et al. (US 6569109).

4. With respect to claim 10, Sakurai discloses a starting-process controller for starting a piezomotor (Fig 3), comprising: a voltage-controlled oscillator (item 17), a power output stage (item 13), a resonance converter (column 9, lines 39-46), a phase comparator (item 15), a phase-locked loop filter (item 16), and an adjustable time-delay element (column 7, line 48 through column 8, line 16), wherein the VCO generates the control signals required for the power output stage (Fig 3), the power output stage provides stepped output voltage (column 9, lines 39-46), the resonance converter converts the stepped output voltage from the power output stage into a motor voltage

for driving the piezomotor (column 9, lines 39-46), the motor voltage being sinusoidal and having an associated motor current when the piezomotor is driven (column 9, lines 39-46), the phase-locked loop filter is configured to smooth the phase-difference signal so as to provide a smoothed signal that controls the VCO (column 13, lines 5-12), and the adjustable time-delay element providing for controlled reduction of the phase difference between the motor voltage and a reference in a start-up process for starting up the piezomotor from an initially large starting angle at initiation of the start-up process towards a smaller operating angle at an operating point, the adjustable time-delay element effecting reduction in the form of one of: (i) a preset linear gradient, the linear gradient having a preset starting delay, a preset final delay, and a preset, fixed change in delay per selected time increment over the duration of the start-up process, such that, at initiation of the start-up process, the starting delay applies to generate a start-up phase angle toward enabling reliable start-up of the piezomotor and, at the operating point, the final delay applies to generate an operating phase angle toward enabling reliable operation of the piezomotor (column 7, line 48 through column 8, line 16), or (ii) ..., or (iii) a preset combination of a linear gradient and a progressive curve.

Sakurai does not disclose expressly that the phase comparator compares the motor current with the phase of the motor voltage, and provides a phase-difference signal representing a measure of the phase difference between motor current and the motor voltage.

Sakurai et al. teaches a controller for a piezoelectric device in which a phase comparator compares the motor current with the phase of the motor voltage, and

provides a phase-difference signal representing a measure of the phase difference between motor current and the motor voltage (column 12, lines 50-55).

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the voltage-current phase comparator of Sakurai et al. with the starting-process controller of Sakurai for the benefit of eliminating the need for the reference signal, thus reducing the number of components required.

5. In order to clarify this rejection, a description of Sakurai, and the interpretation of its teachings as it pertains to the rejections of the claims is provided. Sakurai discloses a control circuit for a piezomotor in which the control circuit monitors the motor current and voltage, compares the phases of the voltage and current, and then adjusts the input signal to compensate for the phase difference between the current and voltage. The objective of Sakurai is to operate the piezomotor with zero phase difference between the motor current and voltage (column 7, line 48 through column 8, line 16). It does this by changing the input signal by a predetermined amount when the motor current and voltage are out of phase (column 7, line 48 through column 8, line 16). When this input signal is changed by the predetermined amount, the phase difference between the motor current and voltage is also being changed by a predetermined amount (Figs 8A-8D). By changing the phase difference between the motor current and voltage, the time-delay between the motor current and voltage is also being changed, as the phase difference and time delay are directly related. As the control circuit of Sakurai creates a time delay by adjusting the phase, Sakurai discloses a time-delay element, this time-delay element being the control circuit itself. The signal of Sakurai is changed

monotonously (column 7, lines 48-68); therefore, the time-delay element effects reduction of the phase difference in a preset linear gradient. In addition, this control process is carried out whenever the device is in operation, including at start-up. At start-up, there will be some phase difference between the motor voltage and current, which can be interpreted as being large. The control circuit of Sakurai will then adjust the phase difference (time-delay), until the phase difference is zero, which is at the operating point.

6. With respect to claim 12, the combination of Sakurai and Sakurai et al. discloses the starting-process controller of claim 10. Sakurai et al. discloses that the adjustable-time delay element comprises a digital counter (item 123), and wherein the digital counter effects the controlled reduction in phase angle between the motor voltage and the motor current in the form of the linear gradient, the progressive curve, or the combination of such gradient and curve (column 12, line 50 through column 13, line 23).

7. With respect to claim 13, the combination of Sakurai and Sakurai et al. discloses the starting-process controller of claim 12. Sakurai et al. discloses that, at selected times during the start-up process, the digital counter has respective starting values such that the starting value of the digital counter at a particular selected time fixes the respective delay as to the motor current, the delay generating a phase angle at such selected time (column 12, line 50 through column 13, line 23).

8. With respect to claim 14, the combination of Sakurai and Sakurai et al. discloses the starting-process controller of claim 13. Sakurai et al. discloses that the digital counter counts from each starting value to a preset final count, the final count being

associated with the passing on of the motor current subject to the respective delay (column 12, line 50 through column 13, line 23).

9. With respect to claim 15, the combination of Sakurai and Sakurai et al. discloses the starting-process controller of claim 13. Sakurai et al. discloses a start-up process delay controller (item 125), the start-up process delay controller controlling the adjustable time-delay element by one or both of (i) providing the starting values to the digital counter of the adjustable time-delay element (column 13, lines 7-9) and/or (ii) having a timing interval associated with the selected time increment between changes in delay.

10. With respect to claim 16, the combination of Sakurai and Sakurai et al. discloses the starting-process controller of claim 10. Sakurai et al. discloses a start-up process delay controller (item 125), the start-up process delay controller controlling the adjustable time-delay element by one or both of (i) providing one or more of the starting delay, the final delay and/or the change in delay (column 13, lines 7-14).

11. With respect to claim 17, the combination of Sakurai and Sakurai et al. discloses the starting-process controller of claim 16. Sakurai et al. discloses that the start-up process delay controller comprises a reference counter that counts oscillations of a reference frequency, the reference frequency forming a clock signal of the reference counter (column 12, line 50 through column 13, line 23).

12. With respect to claim 18, the combination of Sakurai and Sakurai et al. discloses the starting-process controller of claim 17. Sakurai et al. discloses that the counts made

by the reference counter are used directly for setting the delay (column 12, line 50 through column 13, line 23).

13. With respect to claim 19, the combination of Sakurai and Sakurai et al. discloses the starting-process controller of claim 17. Sakurai et al. discloses that the counts made by the reference counter are converted into a value for setting the delay (column 12, line 50 through column 13, line 23).

14. With respect to claim 20, the combination of Sakurai and Sakurai et al. discloses the starting-process controller of claim 17. Sakurai et al. discloses that the counts made by the reference counter are converted into settings for the delay by means of a table of a memory device (item 125 and column 12, line 50 through column 13, line 23).

15. With respect to claim 21, the combination of Sakurai and Sakurai et al. discloses the starting-process controller of claim 10. Sakurai et al. discloses that the starting process is monitored by a programmable control device (item 125).

16. With respect to claim 22, the combination of Sakurai and Sakurai et al. discloses the starting-process controller of claim 21. Sakurai et al. discloses that the programmable control device monitors the phase delay digitally (CPU 125 is a digital computer).

17. With respect to claim 26, Sakurai discloses a starting-process controller for starting a piezomotor (Fig 3), comprising: a voltage controlled oscillator (item 17) adapted to generate a control signal (Fig 3); a power output stage (item 13) adapted to receive the control signal from the VCO (Fig 3) and in response thereto generate a stepped output voltage (column 9, lines 39-46); a resonance converter (column 9, lines

Art Unit: 2834

39-46) adapted to convert the stepped output voltage from the power output stage into a motor voltage for driving the piezomotor (column 9, lines 39-46), the motor voltage being sinusoidal and having an associated motor current when the piezomotor is driven (column 9, lines 39-46); an adjustable time-delay element adapted to delay the motor current by a delay amount (column 7, line 48 through column 8, line 16); a phase comparator (item 15) adapted to output a phase-difference signal representing a measure of a phase difference between the delayed motor current and the motor voltage (Fig 3); and a phase-locked loop filter (item 16) adapted to filter the phase-difference signal and to apply the phase-difference signal to the VCO (Fig 3).

Sakurai does not disclose expressly that the adjustable time-delay element is adapted to receive the motor current or that the phase comparator is adapted to receive the motor voltage and the delayed motor current from the adjustable time-delay element.

Sakurai et al. teaches a controller (Fig 10) for a piezoelectric device in which the time-delay element (item 111) is adapted receive the motor current (Fig 10) and that the phase comparator (item 121) is adapted to receive the motor voltage and the delayed motor current from the adjustable time delay element (Fig 10 and column 12, lines 50-55).

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the voltage-current phase comparator of Sakurai et al. with the starting-process controller of Sakurai for the benefit of eliminating the need for the reference signal, thus reducing the number of components required.

18. In order to clarify this rejection, a description of Sakurai and Sakurai et al., and the interpretations of their teachings as they pertain to the rejections of the claims are provided. The interpretation of Sakurai remains the same as in claim 10 above. In Sakurai et al., the time-delay element is the digital PLL (item 111). Similar to Sakurai, Sakurai et al. effects a time-delay by adjusting the signal, and therefore the phase difference between the voltage and current, with the objective being to drive the piezoelectric device with a phase difference of zero between voltage and current. As can be seen in figure 10 of Sakurai et al., the time-delay element (item 111) receives the motor current from the detection circuit (item 113). The time-delay element then uses this detection signal to make the adjustments to the output signal. This adjustment in the output signal results in a change in the phase difference between voltage and current, which results in an adjustment of the time-delay between the voltage and current. In Sakurai et al., the phase comparator receives the motor voltage from detection circuit (Fig 10). The phase comparator also receives the motor current from the time-delay element, through the power amplifier, as the time-delay of the motor current is not effected by the power amplifier.

Allowable Subject Matter

19. Claims 23-25 and 27-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
20. The following is a statement of reasons for the indication of allowable subject matter: the prior art does not disclose or suggest "wherein an output of the adjustable

time-delay element is directly connected to an input of the phase comparator," or "wherein the adjustable time-delay element delays only one of the motor voltage and the motor current, and provides the delayed one of the motor voltage and the motor current to the input of the phase comparator," or "wherein the adjustable time-delay element includes a binary counter whose output is provided to the input of the phase comparator" in combination with the remaining claim elements of claims 23, 24, and 25 respectively.

Response to Arguments

21. Applicant's arguments filed in the Appeal Brief on 7 January 2008 have been fully considered but they are not persuasive. Applicant argues that Sakurai does not disclose an adjustable time-delay element. However, as described above, Sakurai discloses an adjustable time delay element, as the control circuit of Sakurai adjusts the phase difference between the voltage and current. As the phase difference is related to a time-delay, Sakurai discloses an adjustable time-delay element. Applicant argues that nothing in Sakurai provides for controlled reduction of the phase difference between the motor voltage and motor current in a start-up process for starting from a large starting angle at initiation of the start-up process towards a smaller operating angle at an operating point. However, the primary objective of Sakurai is to decrease the phase difference between motor voltage and current to zero. Sakurai does this throughout operation, including at start-up. Applicant argues that figures 8A-8D show that the phase difference varies periodically. However, this is not the case. Figure 8D shows a graph of phase difference versus frequency, not phase difference versus time. The

primary objective of Sakurai is to use the control circuit to reduce the phase difference between motor voltage and current to zero. Applicant argues that Sakurai does not disclose that the phase difference is reduced in the form of (i) a preset linear gradient, (ii) a preset progressive curve, or (iii) a combination of (i) and (ii). However, Sakurai discloses the phase difference being adjusted monotonously (column 7, lines 48-68). This results in a preset linear gradient. In addition, any form taken by the change in phase difference could be described as at least one of (i), (ii), or (iii). Applicant argues that the combination of Sakurai and Sakurai et al. is improper, as it is not supported by objective evidence in the record. However, the reason for combining Sakurai and Sakurai et al. has been provided as "for the benefit of eliminating the need for the reference signal, thus reducing the number of components required". The control circuit of Sakurai includes a reference signal generating circuit as part of its control circuit (Fig 3). The need for this component is eliminated in Sakurai et al. (Fig 1). Therefore, at the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the voltage-current phase comparator of Sakurai et al. with the starting-process controller of Sakurai for the benefit of eliminating the need for the reference signal, thus reducing the number of components required. Applicant also argues that the VCO PLL and the DDS circuits are not compatible. However, a DDS and VCO are simply alternative means of generating controlled signals in a digital environment, with a VCO being capable of being used in either a digital or analog control circuit.

22. Applicant's arguments with respect to claim 26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Akahane et al. (US 2002/0171410) discloses a piezoelectric control circuit in which a VCO is used as part of a digital control circuit (Fig 28).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Derek J. Rosenau whose telephone number is (571)272-8932. The examiner can normally be reached on Monday thru Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Darren Schuberg can be reached on 571-272-2044. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Derek J Rosenau
Examiner
Art Unit 2834

Art Unit: 2834

/D. J. R./

Examiner, Art Unit 2834

/Darren Schuberg/

Supervisory Patent Examiner, Art Unit 2834